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Notice of Allowability	Application No.	Applicant(s)	
	10/781,746	MIYAMOTO ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 9/12/05*.

2. ☒ The allowed claim(s) is/are *2-7,9-13,15,16 and 18-20*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *9/22/05* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Gregory E. Montone on 9/22/05.

The application has been amended as follows:

Claim 16. (Currently Amended) The semiconductor integrated-circuit device comprising: one or more logic gates between an output of a first flip-flop and an input of a second flip-flop;

wherein part of said plurality of logic gates is constituted by a depletion-type MOSFET; and

wherein the logic gates in said semiconductor integrated circuits are further formed with first MOSFETs of the enhancement type whose threshold voltage is a first threshold voltage, and second MOSFETs of the enhancement type whose threshold voltage is a second threshold voltage, said first threshold voltage being higher than said second threshold voltage; and

further comprising input/output circuits for exchanging signals with external terminals, wherein said input/output circuits are constituted by a plurality of MOSFETs having said first threshold voltage, and said plurality of MOSFETs are MOSFETs different in withstand voltage.

Claim 17. (Cancelled)

2. The following is an examiner's statement of reasons for allowance: in combination with other limitations of the claims, the cited prior arts fail to teach the depletion-type MOSFET constituting the logic gate circuit to be replaced is formed by applying a manufacturing step for depletion to a MOSFET having the same pattern and size as those of the enhancement type MOSFET that has not been replaced, as recited in amended claim 2; the cited prior arts also fail to teach the flip-flop circuits and the first signal transferring path are constituted by the enhancement-type MOSFETs with high threshold voltage; and wherein the second signal transferring path is constituted by the enhancement-type MOSFETs with high threshold voltage and the enhancement- type MOSFETs with low threshold voltage, by the enhancement-type MOSFETs with low threshold voltage, by said enhancement-type MOSFETs with low threshold voltage and the depletion-type MOSFETs, or by the depletion-type MOSFEts, as recited in amended claim 3; the cited prior arts also fail to teach wherein the third step is followed by the second step after, of all the enhancement-type MOSFETS constituting the signal transferring paths, a MOSFET having a maximum delay time has been replaced with the depletion-type MOSFET, as recited in amended claim 9; and the cited prior arts also fail to teach the logic gates in the semiconductor integrated circuits are further formed with first MOSFETs of the enhancement type whose threshold voltage is a first threshold voltage, and second MOSFETs of the enhancement type whose threshold

voltage is a second threshold voltage, the first threshold voltage being higher than the second threshold voltage, as recited in amended claims 15 and 16.

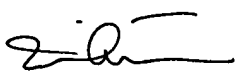
3. Claims 2-7, 9-13, 15, 16, and 18-20 are now in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



VIBOL TAN
PRIMARY EXAMINER